Fig.1

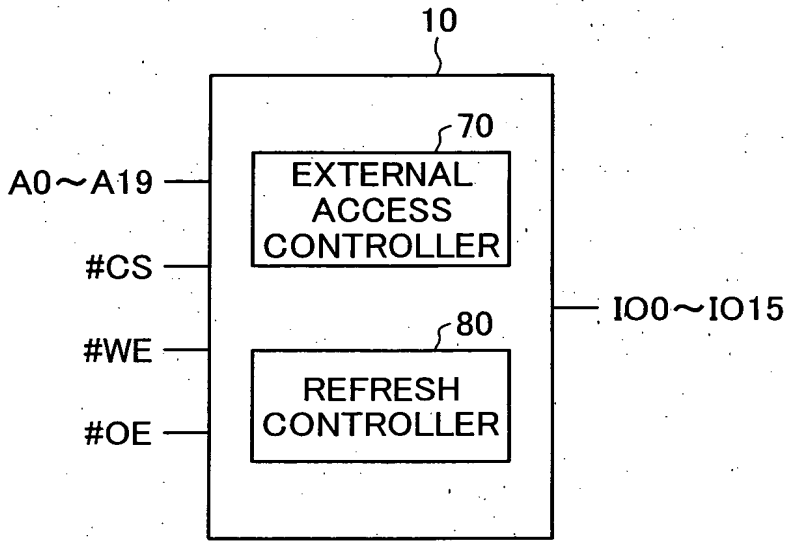


Fig.2

	#CS	REFRESH MODE (*)
OPERATION	L	MODE 1
STAND-BY	H	MODE 2

(*)

Refresh Mode 1: The refreshing operation starts synchronously with the output enable signal or the write enable signal after the generation of the refresh timing signal in the memory chip.

Refresh Mode 2: The refreshing operation starts according to the generation of the refresh timing signal in the memory chip (address input is not required).

Fig.3

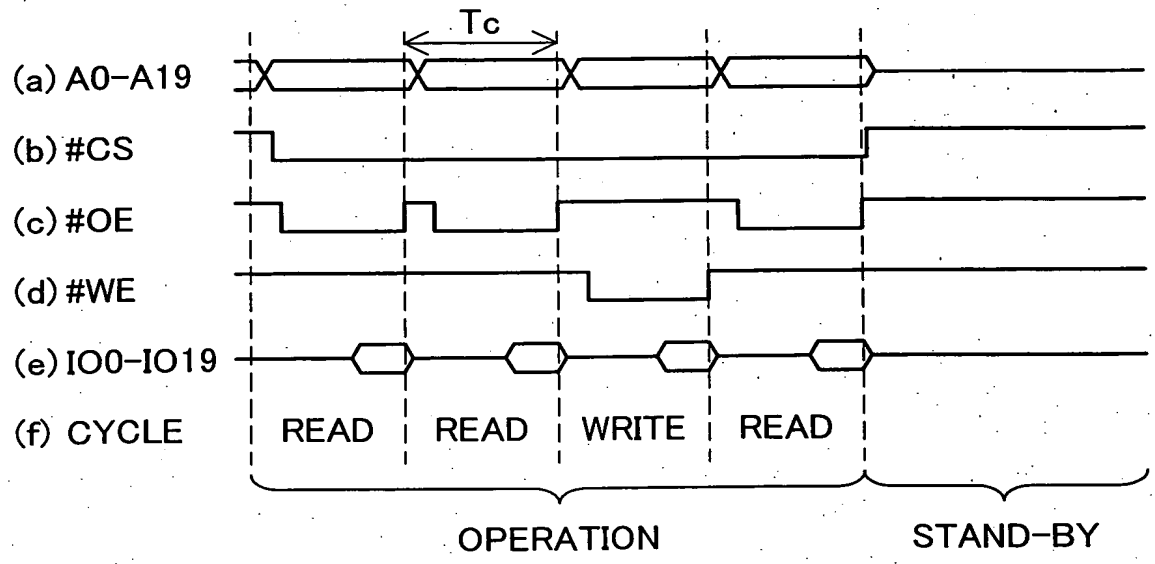

Tc
(a) A0-A19
(b) #CS
(c) #OE
(d) #WE
(e) IO0-IO19
(f) CYCLE
READ
READ
WRITE
READ
OPERATION
STAND-BY

Fig.4

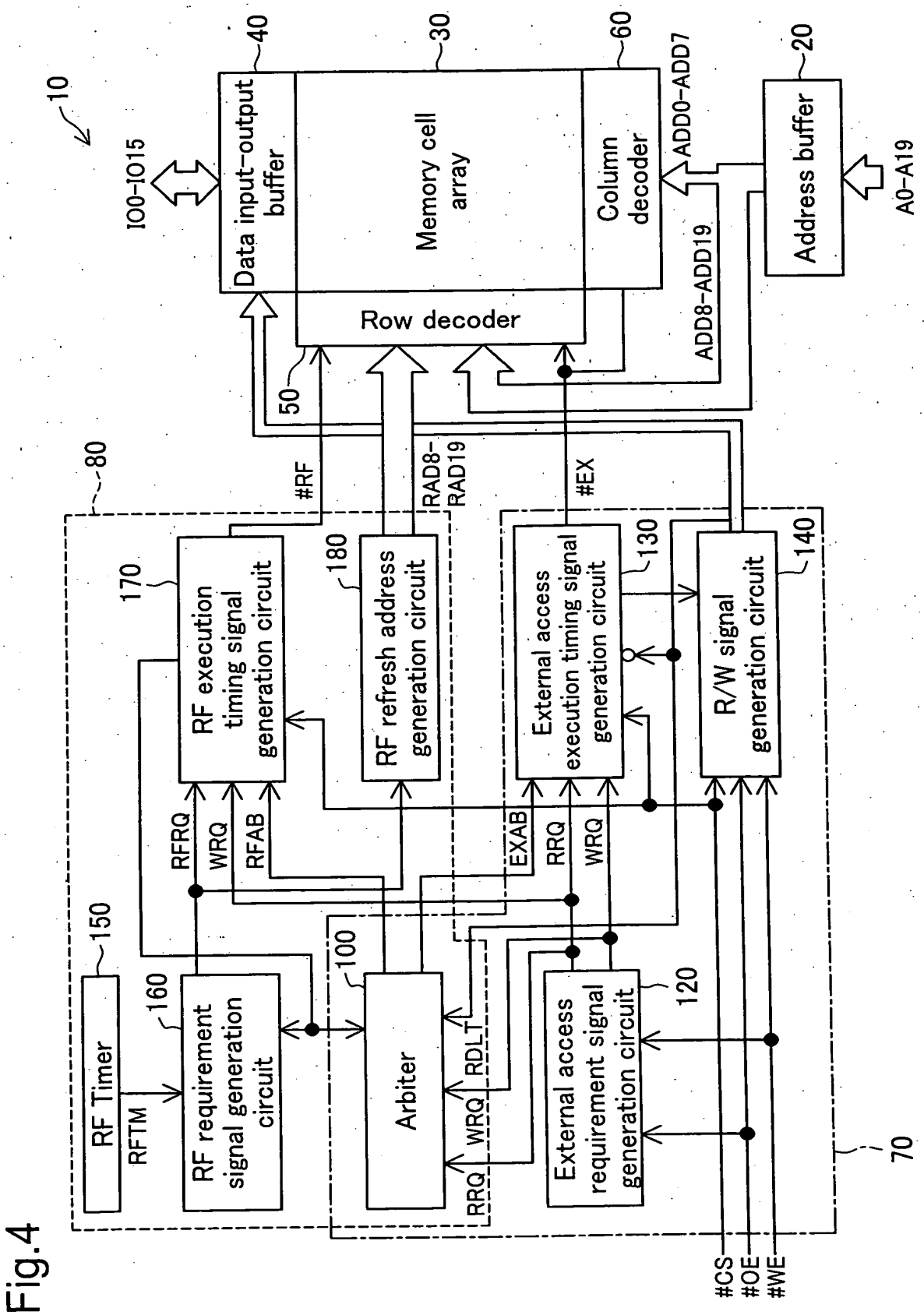

10
I00-I015
Data input-output buffer
40
Memory cell array
30
Column decoder
60
ADD0-ADD7
Address buffer
20
A0-A19
Row decoder
50
ADD8-ADD19
80
#RF
RAD8-RAD19
#EX
RF execution timing signal generation circuit
170
RF refresh address generation circuit
180
External access execution timing signal generation circuit
130
R/W signal generation circuit
140
RFRQ
WRQ
RFAB
EXAB
RRQ
WRQ
150
RF Timer
RFTM
160
RF requirement signal generation circuit
100
Arbiter
RDLT
WRQ
RRQ
External access requirement signal generation circuit
120
70
#CS
#OE
#WE

Fig.5

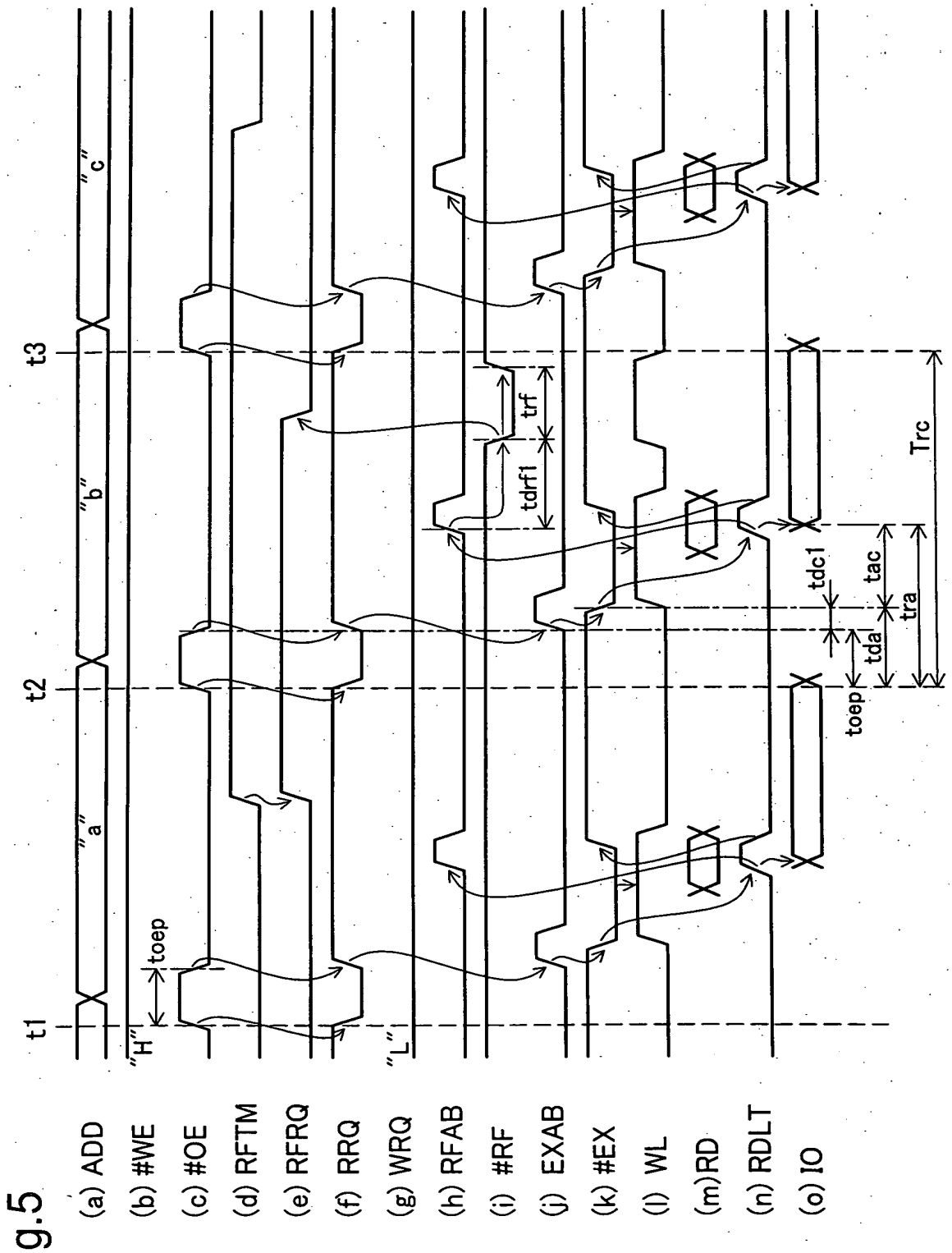

(a) ADD
(b) #WE
(c) #OE
(d) RFTM
(e) RFRQ
(f) RRQ
(g) WRQ
(h) RFAB
(i) #RF
(j) EXAB
(k) #EX
(l) WL
(m)RD
(n) RDLT
(o) IO
t1
t2
t3
"a"
"b"
"c"
"H"
"L"
toep
tdrf1
trf
tdc1
tac
tra
tda
toep
Trc

Fig.6

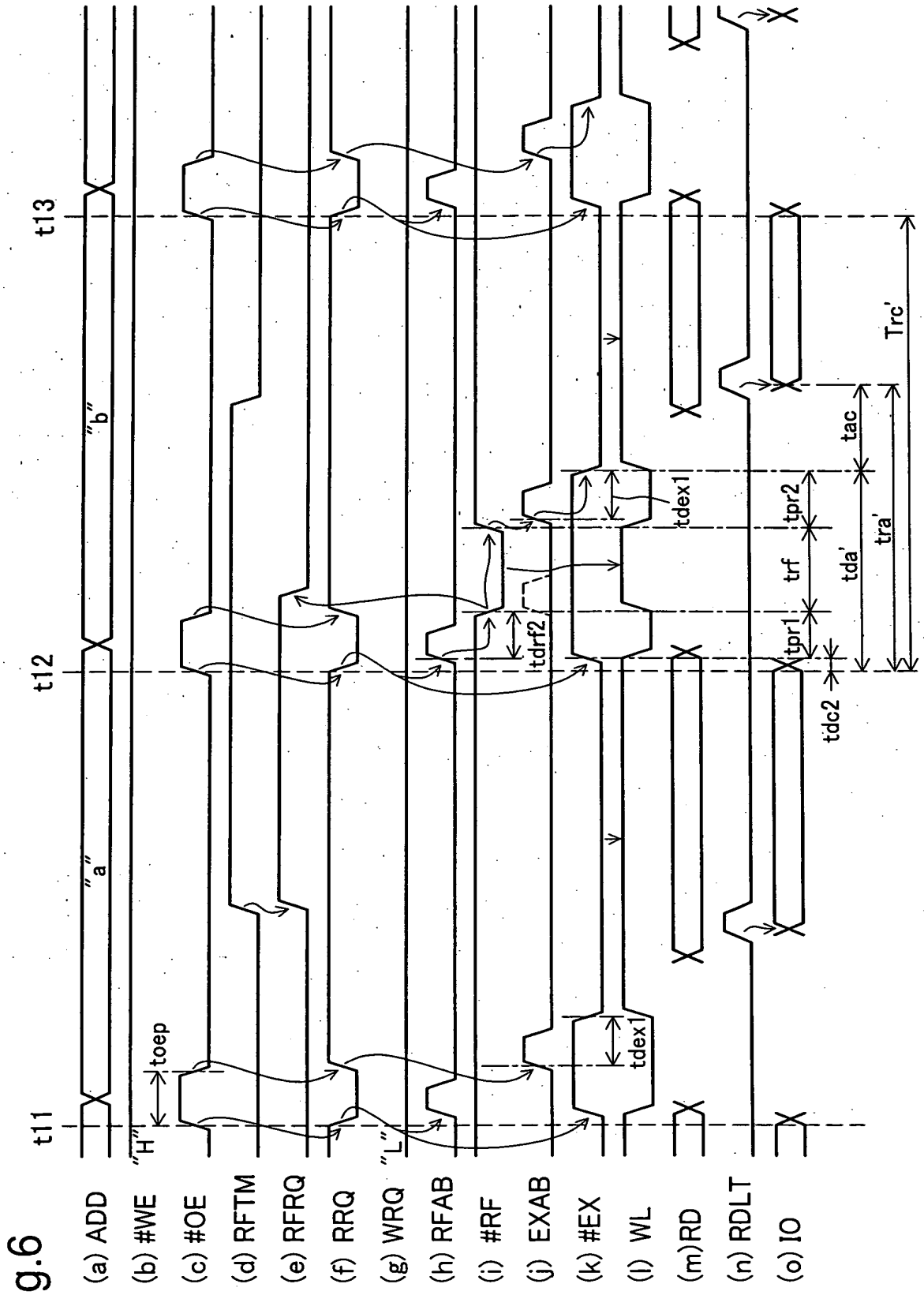
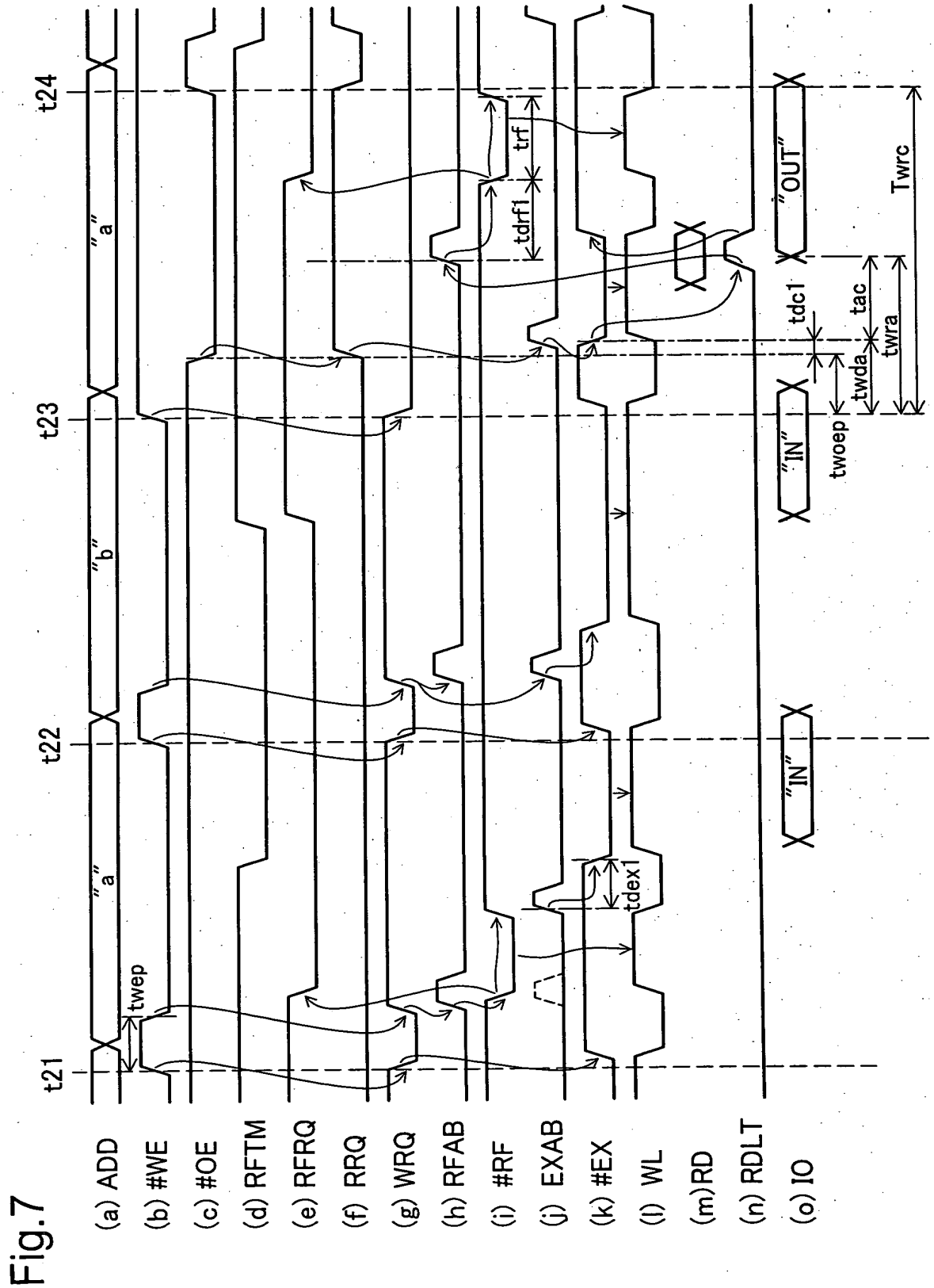

t11
t12
t13
(a) ADD
(b) #WE
(c) #OE
(d) RFTM
(e) RFRQ
(f) RRQ
(g) WRQ
(h) RFAB
(i) #RF
(j) EXAB
(k) #EX
(l) WL
(m)RD
(n) RDLT
(o) IO
"a"
"b"
"H"
"L"
toep
tdex1
tdrf2
tdex1
tac
tpr2
trf
tpr1
tda'
tra'
Trc'
tdc2

Fig.7


t21
t22
t23
t24
(a) ADD
(b) #WE
(c) #OE
(d) RFTM
(e) RFRQ
(f) RRQ
(g) WRQ
(h) RFAB
(i) #RF
(j) EXAB
(k) #EX
(l) WL
(m)RD
(n) RDLT
(o) IO
"a"
"b"
"a"
twep
tdex1
trf
tdrf1
"IN"
"IN"
"OUT"
tdc1
tac
twra
twda
twoep
Twrc

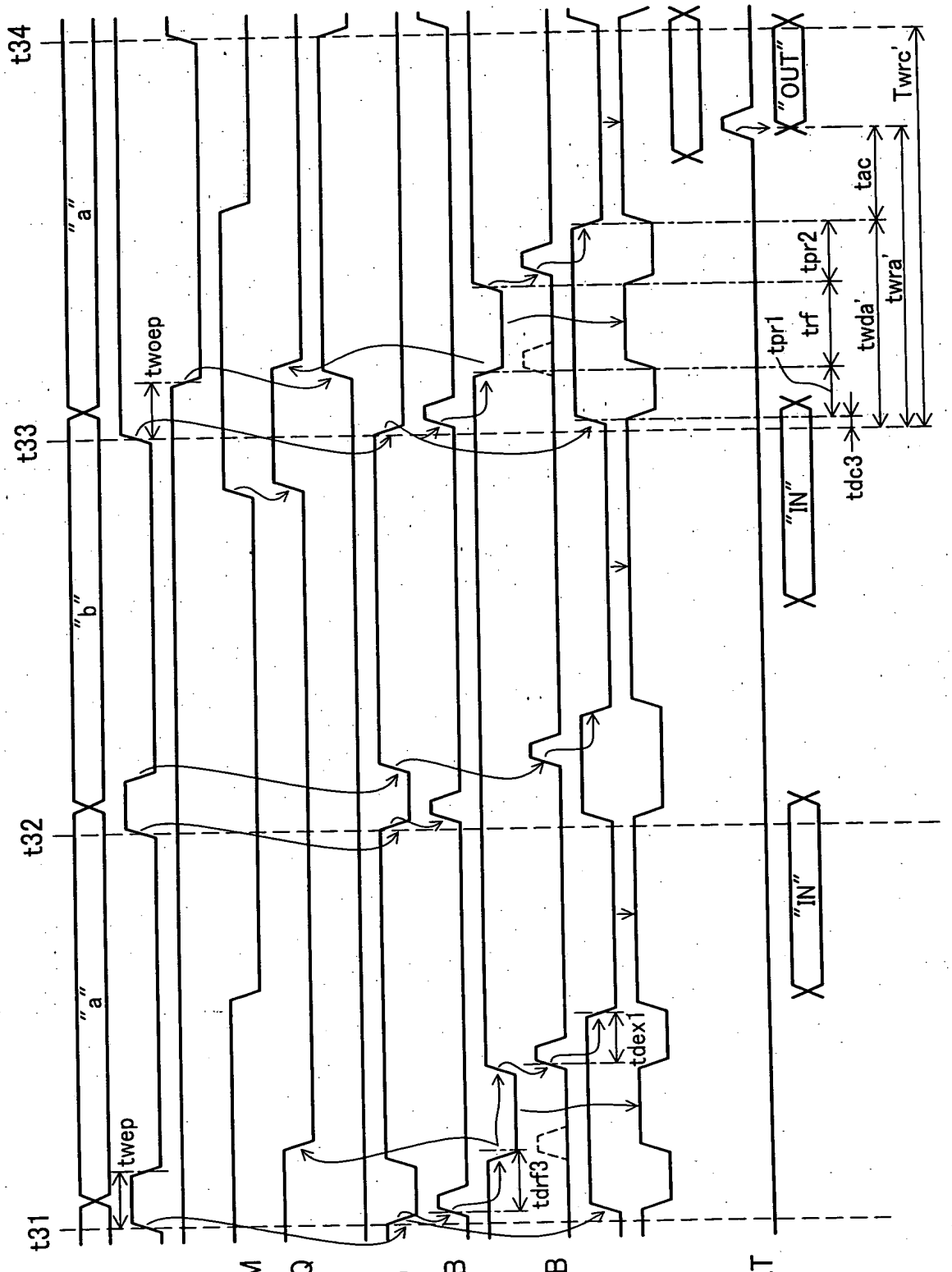

t31
t32
t33
t34
(a) ADD
(b) #WE
(c) #OE
(d) RFTM
(e) RFRQ
(f) RRQ
(g) WRQ
(h) RFAB
(i) #RF
(j) EXAB
(k) #EX
(l) WL
(m) RD
(n) RDLT
(o) IO
"a"
"b"
"a"
twep
twoep
tdrf3
tdex1
"IN"
"IN"
"OUT"
tpr1
trf
tpr2
tdc3
twda'
twra'
tac
Twrc'

Fig.8

Fig.9

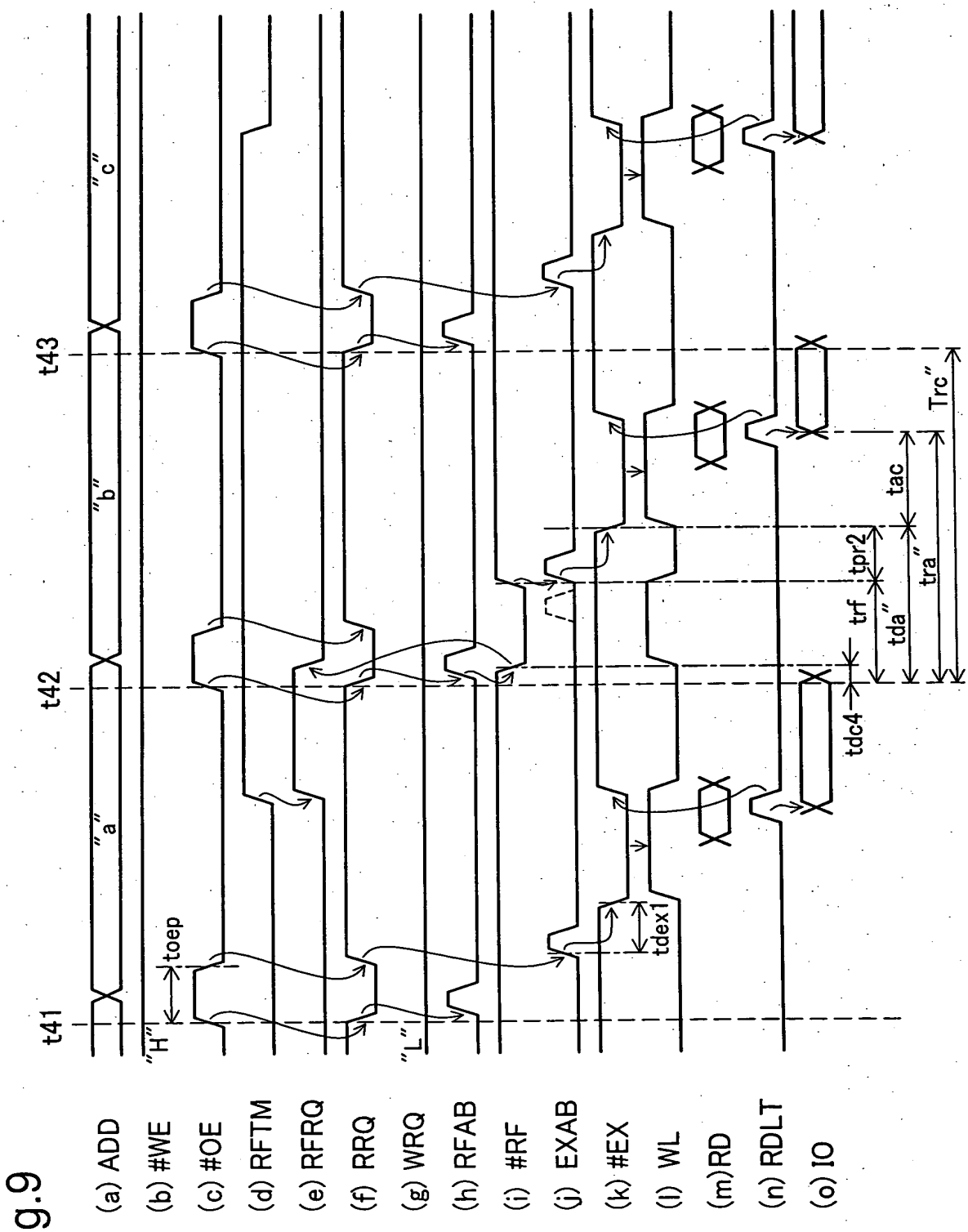

(a) ADD
(b) #WE
(c) #OE
(d) RFTM
(e) RFRQ
(f) RRQ
(g) WRQ
(h) RFAB
(i) #RF
(j) EXAB
(k) #EX
(l) WL
(m)RD
(n) RDLT
(o) IO
t41
t42
t43
"a"
"b"
"c"
"H"
"L"
toep
tdex1
tdc4
trf
tpr2
tac
tda"
tra"
Trc"

Fig.10

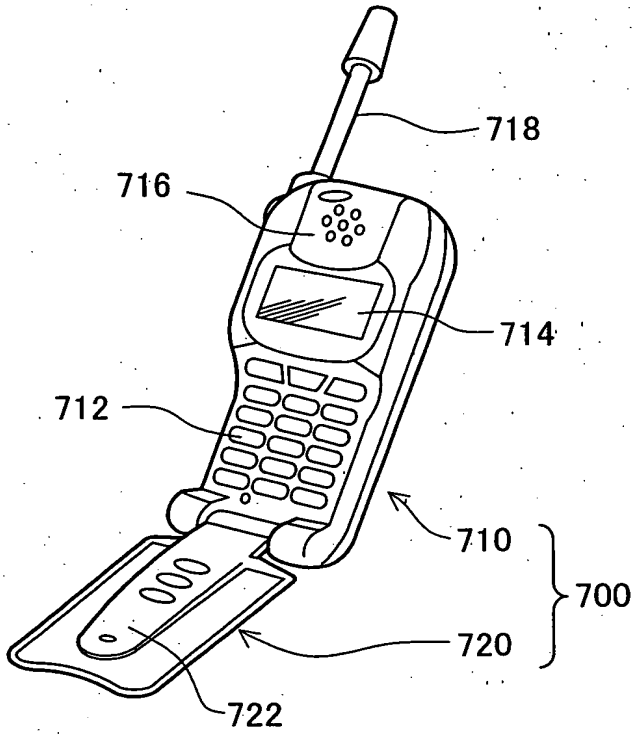
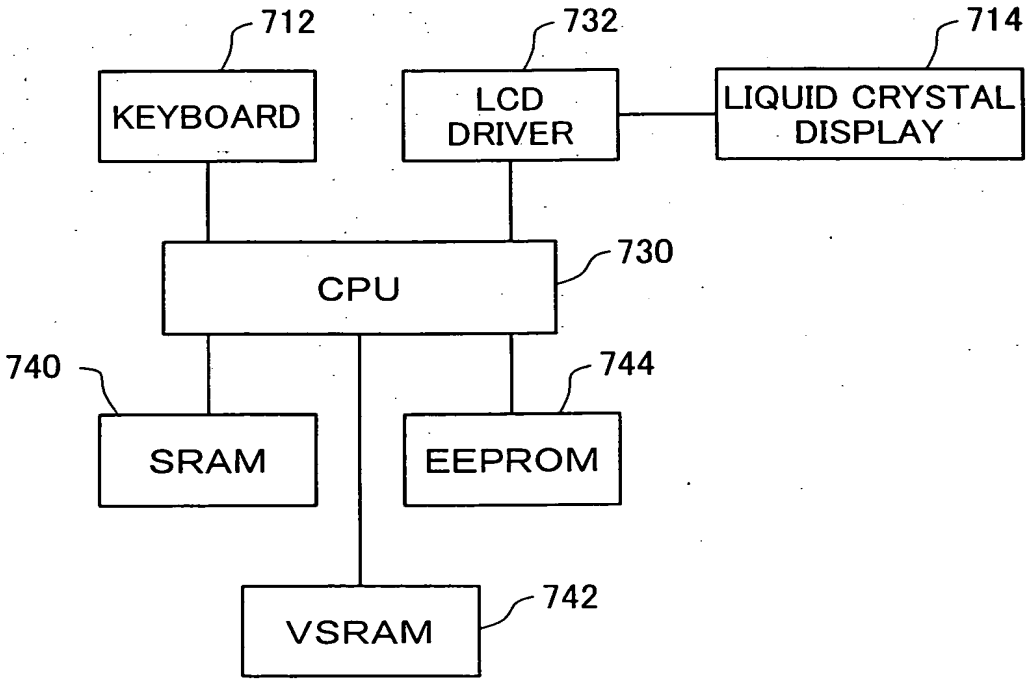

718
716
714
712
710
700
720
722

Fig.11


712
KEYBOARD
732
LCD DRIVER
714
LIQUID CRYSTAL DISPLAY
CPU
730
740
SRAM
744
EEPROM
VSRAM
742